REMARKS

Fig. 6 has been objected to for not including a legend such as -Prior Art-. However, the delay lock loop 600 of Fig. 6 includes a connection to provide a synchronization signal SYNCH_CLK to a digital frequency synthesizer in accordance with one embodiment of the present invention.

Applicants do not believe that this element of Fig. 6 is prior art. If the Examiner believes that this element is prior art, the Examiner is required to show a prior art reference that discloses this element. For these reasons, Applicants are not amending Fig. 6 at this time.

The Examiner has objected to the phrase "substantially equal to" in Claims 6 and 11. Claims 6 and 11 recite "wherein the DLL output delay is substantially equal to the DFS output delay".

A phrase such as "substantially equal to" can be definite if it be shown that a person of skill in the art would understand the limitation. Seattle Box Co. v. Industrial Crat. & Pack., Inc., 731, F.2d 818, 221 USPQ 568 (Fed. Cir. 1984). In the present case, a person of ordinary skill would be able to select a DLL output delay "substantially equal to" a DFS output delay in view of Applicant's teachings, which indicates that "the components of DFS output circuit 324 and DLL output circuit 314 are chosen to match DLL output delay 316 with DFS output delay 326", such that the "frequency adjusted clock signal FREQ_CLK can be synchronized with output clock signal O_CLK". (Specification, page 12, lines 15-24.) For this reason, Claims 6 and 11 are not being amended at this time.

Claims 1, 2, 4 and 5 have been rejected under 35 U.S.C. 102(e) as being anticipated by Hassoun (U.S. Patent No. 6,487,648).

Claim 1 recites "a delay lock loop" and "a digital frequency synthesizer, coupled to the delay lock loop".

The Examiner states "as shown in Figure 4, Hassoun discloses a digital clock manager … comprising: a delay lock

loop (DLL) (304B) … and a digital frequency synthesizer (304A), coupled to the delay lock loop".

However, contrary to the Examiner's assertions, element 304A of Hassoun is not a digital frequency synthesizer, but rather, a delay lock loop that provides "a standard clock signal". (Hassoun, Col. 9, lines 62-66; Fig. 4.)

Thus, Hassoun fails to teach or suggest a digital frequency synthesizer as recited by Claim 1. For this reason, Claim 1 is not anticipated by Hassoun. Claims 2, 4 and 5, which depend from Claim 1, are not anticipated by Hassoun for at least the same reasons as Claim 1.

Claims 3, and 6-18 have been objected to as being dependent upon a rejected base claim. The Examiner has indicated that these claims would be allowable if rewritten in independent form, including all of the limitations of the base claim and any intervening claims. However, because Applicants believe that the base claims are allowable (for reasons stated above), Applicants are not amending Claims 3 and 6-18 at this time.

Applicants note with appreciation the allowance of Claims 19-22.

The specification at page 14, lines 22-36 has been amended to correct the status information of the citation.

CONCLUSION

Claims 1-22 are pending in the present application. Reconsideration of Claims 1, 2, 4 and 5 is requested.

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

If there are any questions, the applicants' attorney can be reached at Tel: 408-879-6149 (Pacific Standard Time).

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as FIRST CLASS MAIL in an envelope addressed to: Mail Stop Non-Fee Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on March 17, 2004..

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